

Fig. 1
(Prior Art)

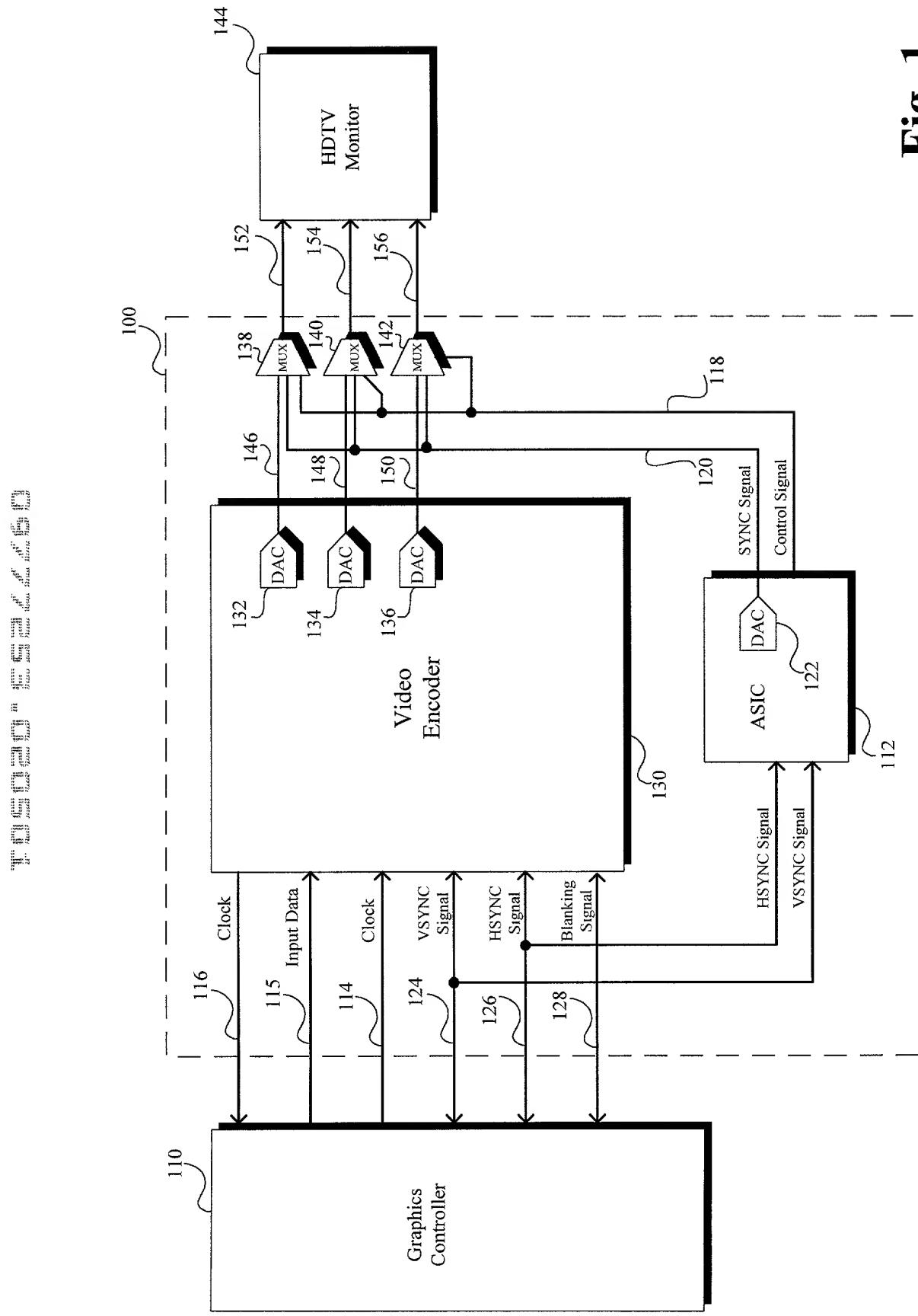


Fig. 2

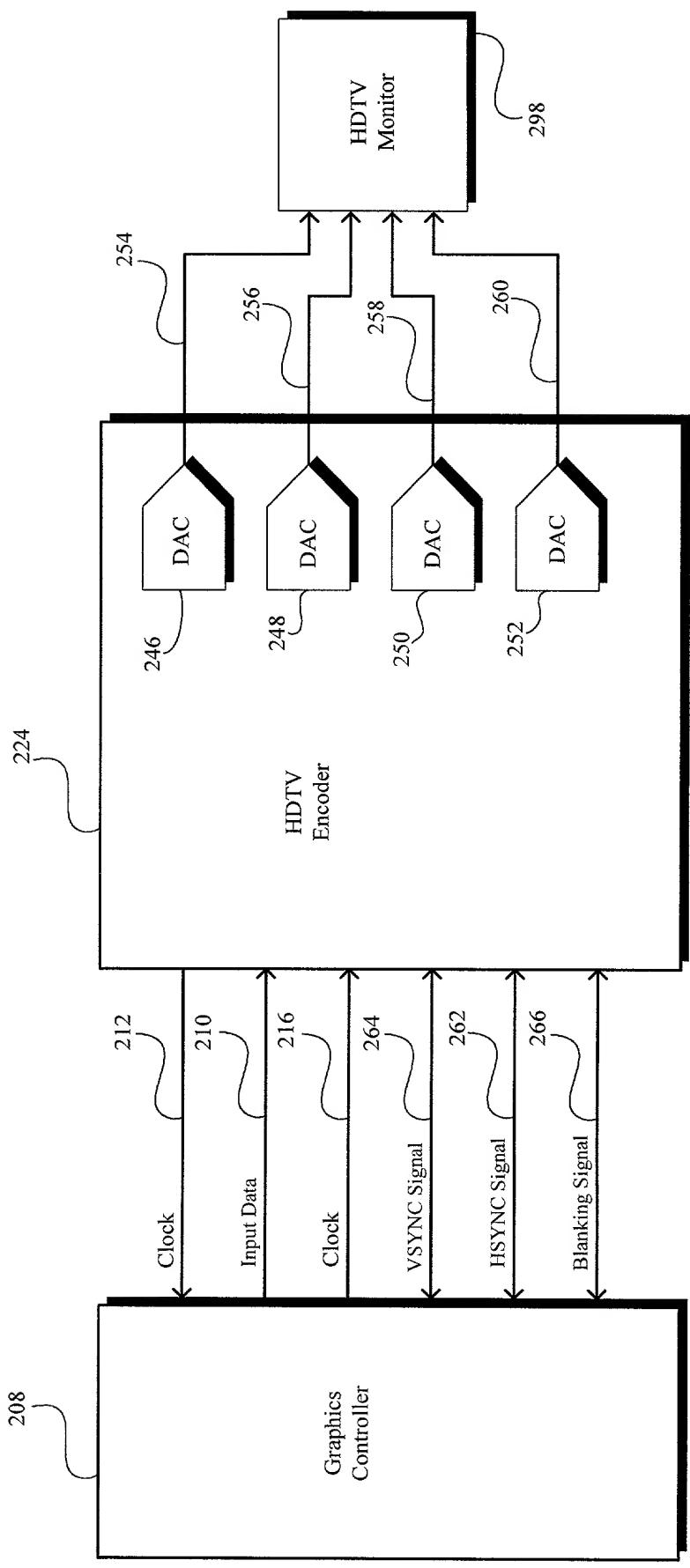


Fig. 3

Input Data
HSYNC Signal
VSYNC Signal
Blanking Signal

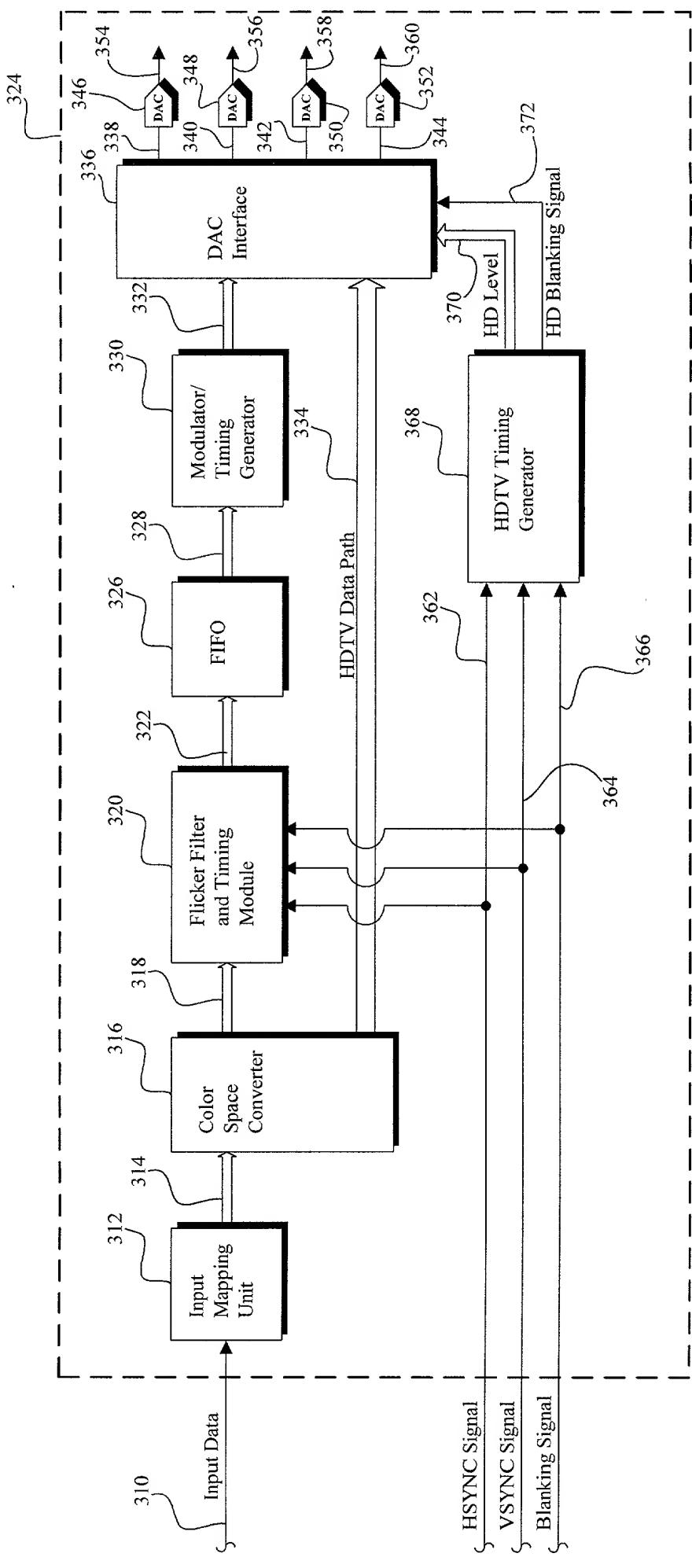


Fig. 4

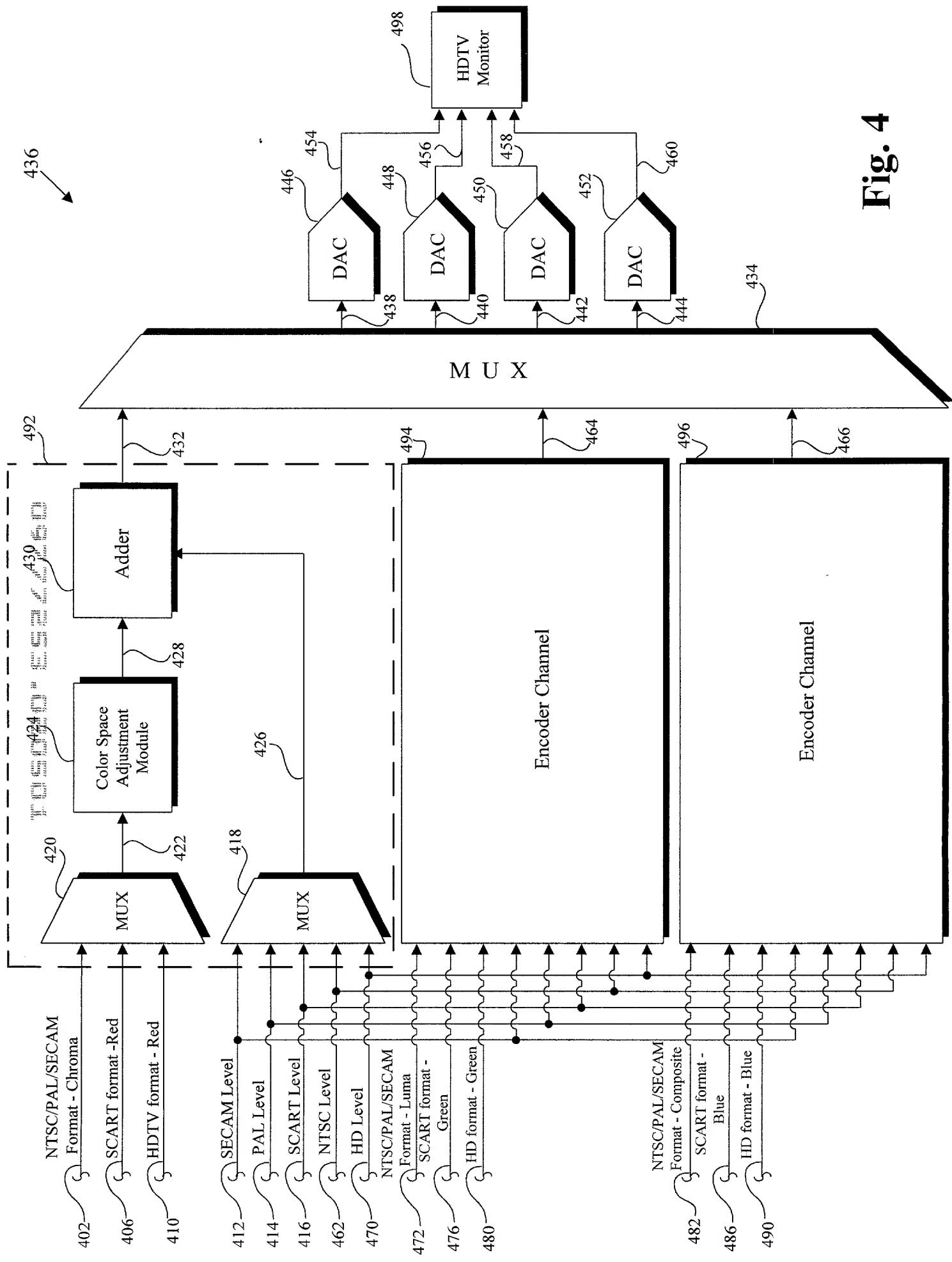


Fig. 5